UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,855	09/29/2000	Gary Dan Dotson	00AB147 (81696/235)	9316

7590   02/27/2003

Rockwell Technologies, LLC
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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *14 November 2000* .

2a) ☐ This action is **FINAL.**   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) *11-21* is/are allowed.

6) ☒ Claim(s) *1-10* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *29 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____ .

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4)

because reference character "27" in Figure 1 has been used to designate both SRAM &

Flash Interface and SDRAM Interface and reference character "70" in Figure 4 has been

used to designate DMA Controller 0, DMA Controller 1 and DMA Controller 2^N-1. A

proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not

be held in abeyance.

2.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4)

because reference characters "60-0" and "60" in Figure 2 have both been used to

designate "Resource 0" (if "60" is meant to refer to all Resource Blocks collectively, it

should be drawn that way). A proposed drawing correction or corrected drawings are

required in reply to the Office action to avoid abandonment of the application. The

objection to the drawings will not be held in abeyance.

3.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4)

because reference characters "70-0" in Figure 2 and "70" in Figure 4 have both been

used to designate "DMA Controller 0"; and "70-1" in Figure 2 and "70" in Figure 4 have

both been used to designate "DMA Controller 1". A proposed drawing correction or

corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4.   The drawings are objected to because the handwritten symbols in the drawings are difficult to decipher in places. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: '70-M' in line 23 of page 6 and '218' in line 23 on page 20. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6.   The Examiner would like to point out that the drawing are replete with drawing errors some of which have been pointed out above. The Applicant should review and revise the drawings to remove all drawing errors.

Specification

7.   The disclosure is objected to because of the following informalities: '70-M' in line 23 of page 6 and '218' in line 23 on page 20 are not found in the drawings.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8.   Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Wolf,

Tod (US 6385751 B1).

35 U.S.C. 103(a) rejection of claim 1.

Wolf teaches a system comprising: an arithmetic unit, the arithmetic unit being coupled

to receive data from a general purpose DMA controller (see Reed-Solomon

Coprocessor in Figures 4 and 5 with Encoder 457 and Decoder 458 in Figure 4 of Wolf,

Note: in col. 2, lines 32-35 Wolf teaches that Reed-Solomon encoders/decoders use

Finite Field arithmetic called Galois Field arithmetic hence Reed-Solomon

encoders/decoders are arithmetic units, in particular, the Reed-Solomon Coprocessor in

Figures 4 and 5 is an arithmetic unit; in col. 8, lines 63-64, Wolf teaches that the Reed-

Solomon decoder part of the Reed-Solomon Coprocessor is designed to receive data

from a general purpose DMA controller), the arithmetic unit generating an error

checking value based on the data received from the general purpose DMA controller and based on a polynomial equation (Reed-Solomon decoders inherently generate error checking values based on a polynomial equation, see col. 3, lines 24-27 and col. 5, lines 16-26 in Wolf; in addition, in col. 8, lines 30-31, Wolf teaches that data is received from the DMA).

Note: in col. 6, lines 37-40, Wolf teaches that the Reed-Solomon Coprocessor is implemented as embedded circuitry; hence he Reed-Solomon Coprocessor is an arithmetic **circuit**. Note: in col. 20, lines 49-53, Wolf teaches that the DSP in Figure 6 is used to implement the function of a DMA controller that is to provide general control functions for the purpose of accessing memory, hence the DSP in Figure 6 of Wolf is a general purpose DMA [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 2.

Wolf teaches that the Reed-Solomon Coprocessor uses a generator polynomial $\gamma(x)$ to create different generator polynomials $\gamma(x)$ by varying j_0 {see col. 3, lines 24-46, Wolf}. Note: the Reed-Solomon decoder must use the same generator polynomials $\gamma(x)$ in order to generate syndromes (col.4, lines 59-66,, wolf) which are defined as the remainder derived by dividing the received codeword by the generator polynomial.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

9.   Claims 3-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Wolf, Tod (US 6385751 B1) in view of McSpadden, Jeff R. (US 4216540 A).

35 U.S.C. 103(a) rejection of claim 3.

Wolf, substantially teaches the claimed invention described in claims 1 and 2 (as

rejected above).

However Wolf, does not explicitly teach the specific use of a linear feedback shift

register capable of being modified based on a particular generator polynomial.

McSpadden, in an analogous art, teaches a linear feedback shift register capable of

being modified based on a particular generator polynomial (see Figure and Abstract in

McSpadden, specifically, see feedback control 28 in McSpadden). The Examiner would

like to point out that Wolf teaches an arithmetic unit that requires use of a means,

capable of being modified according to a specific generator polynomial, for generating

code and syndromes based on the specific generator polynomial. One of ordinary skill

in the art at the time the invention was made would have recognized the McSpadden

provides the means necessary to implement the arithmetic unit in McSpadden.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Wolf with the teachings of McSpadden by including a

linear feedback shift register capable of being modified based on a particular generator

polynomial. This modification would have been obvious to one of ordinary skill in the

art, at the time the invention was made, because one of ordinary skill in the art would

have recognized that a linear feedback shift register capable of being modified based on

a particular generator polynomial would provide the opportunity to implement the

arithmetic unit in McSpadden by providing a specific element required in the teaching of

McSpadden for implementing the Arithmetic unit in McSpadden.

35 U.S.C. 103(a) rejection of claim 4.

See 12 in the Figure in McSpadden.

35 U.S.C. 103(a) rejection of claim 5.

Shift registers 22 along with accompanying circuitry such as multiplexers 12 in

McSpadden comprise programmable shift registers.

35 U.S.C. 103(a) rejection of claim 6.

The polynomials cited in claim 6 are the result of selecting appropriate "Galois Field"

parameters (see col. 2, lines 30-31, Wolf).

35 U.S.C. 103(a) rejection of claim 7.

Wolf teaches Reed-Solomon encoders/decoders use Finite Field arithmetic, which is

sometimes called Galois Field arithmetic and includes addition, multiplication, **division**

(col. 2, lines 32-34, Wolf) [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 8.

Reed-Solomon Code is Cyclic code, hence a Systematic Reed-Solomon code is a CRC

code. In column 3, line 30, Wolf teaches how to generate a Systematic Reed-Solomon

code, i.e., a CRC code.

35 U.S.C. 103(a) rejection of claim 9.

See polynomial generator in column 3, lines 35-36 in Wolf. Note: in Wolf the design

requires a setup register (col. 8, lines 24-25, Wolf) which requires j0 in the polynomial

generator in column 3, lines 35-36 in order to implement the design in Wolf.

35 U.S.C. 103(a) rejection of claim 10.

See DSP in Figure 5. Note: a DSP is **capable** of controlling DMA communications to

peripheral devices [Emphasis Added].

Allowable Subject Matter

10.   Claims 11-21 allowed.

The following is an examiner's statement of reasons for allowance:

The present invention pertains to a method and an apparatus for generating different codewords based on generating polynomials using programmable circuitry to implement polynomial operations. Claim 59 recites various features: "(B) a linear feedback shift register, the linear feedback shift register being coupled to receive data from the general purpose DMA controller, the linear feedback shift register comprising a plurality of programmable polynomial building blocks, the plurality of programmable polynomial building blocks being connected in a sequence with each building block corresponding to a respective exponential term in a polynomial of a polynomial equation implemented by the linear feedback shift register, each building block comprising

(1) a feedback gate, the feedback gate being coupled to an output of an adjacent polynomial building block in the sequence and to a non-adjacent polynomial building block in the sequence,

(2) a multiplexer, the multiplexer being coupled to an output of the feedback gate and to the output of the adjacent polynomial building block in the sequence, the multiplexer determining whether the flip flop receives an input from an output of the feedback gate or from the output of the adjacent polynomial building block,

(3) a flip flop, the flip flop having an input coupled to an output of the multiplexer, and wherein, when the flip flop receives an input from the output of the feedback gate, the respective exponential term is included in the polynomial; wherein, when the flip flop receives an input from the immediately preceding flip flop, the respective exponential term is not included in the polynomial; and wherein the multiplexers of each of the

programmable polynomial building blocks are programmable to determine which of the

exponential terms are included in the polynomial of the polynomial equation".

The Prior Art of record teach methods and apparatus for generating different codewords

based on generating polynomials using programmable circuitry implement polynomial

operations and specifically McSpadden teaches a circuit capable of implementing a

programmable linear feedback shift register capable of being modified based on a

particular generator polynomial however, there is no obvious reason why or how the

circuit in McSpadden could be modified to implement the specific details and functions

of the circuit taught in the current application. Hence the prior art taken alone or in any

combination fail to teach the claimed novel feature in claim 11.

Claims 12-21 depend from claim 11, hence are also allowed.

Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany

the issue fee. Such submissions should be clearly labeled "Comments on Statement of

Reasons for Allowance."

Conclusion

11.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Graham, Randolph H. et al. (US 4819153 A) teaches use of a

programmable ECC. Harrison, Joel N. et al. (US 4639863 A) teaches use of a
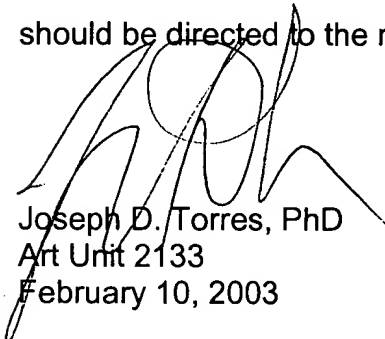
programmable ECC. Sato, Fumitaka (US 4604748 A) teaches a Programmable DMA

Controller and a universal polynomial generator.

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Joseph D. Torres whose telephone number is (703)

308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 746-7239

for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
February 10, 2003

ALBERT DECADY
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